REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the pending application. The Final Office Action dated November 24, 2010 has been received and its contents carefully reviewed.

By this Response, claims 1, 7, 10 and 24 are amended. Claims 3 and 21-22 have previously been canceled, and claims 9 and 12-20 have previously been withdrawn. Accordingly, claims 1-2, 4-8, 10-11 and 23-24 are pending for consideration.

In the Office Action, claims 1, 2, 4-8, 10-11, and 23-24 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,748,266 to Kodate (hereinafter "Kodate") in view of U.S. Patent No. 6,862,050 to Rho et al. (hereinafter "Rho") and U.S. Patent No. 6,204,907 (hereinafter "Hiraishi"). The rejection is respectfully traversed.

With regard to independent claim 1, as amended, Applicant respectfully submits that none of cited references teaches or suggests whole technical feature of claim 1. In particular, the cited references fail to teach at least the features of "…wherein a distance between the pixel electrode in the pixel region and the common electrode is substantially the same as the thickness of the seal pattern".

In figure 8 of Kodate, a distance between a pixel electrode (10) in the pixel region and a common electrode (30) is smaller than a thickness of a seal pattern (64). In addition, since an interlayer insulating layer (9), for example, in figure 2 of Hiraishi, is disposed under a pixel electrode (4), a distance between the pixel electrode (4) in the pixel region and a common electrode (6) is also smaller than a thickness of a seal pattern (14).

Hiraishi discloses at column 9, line 66 to column 10, line 8:

> "First, TFT substrate 10 is manufactured in the same manner as in the first embodiment. Then as shown in FIG. 2, a part of an interlayer insulating film 9 under a seal 14 is removed during patterning of the interlayer insulating film 9. Therefore, gate wirings 1 and a gate insulating film 5 formed on the gate wirings 1 are provided on a transparent insulating substrate 11 below the seal 14. *The interlayer insulating film 9 and a pixel electrode 4 are stacked on the gate wirings 1 and gate insulating film 5 on the transparent insulating substrate 11 inside the seal 14.*"

Namely, neither Kodate nor Hiraishi teach or suggest the claimed invention including a feature of "…wherein a distance between the pixel electrode in the pixel region and the common electrode is substantially the same as the thickness of the seal pattern." Additionally, Rho fails to remedy the deficiencies. Accordingly, Applicant respectfully submits claim 1 and claims 2 and 4-6, which are dependent from claim 1, are allowable over the cited references.

For similar reasons set forth above, Applicant respectfully submits none of the cited reference discloses the above features of amended independent claims 7, 10 and 24. In addition, claim 8, which is dependent from claim 7, and claims 11 and 23, which are dependent from claim 10, are allowable over the cited references.

Applicants believe the foregoing amendments and remarks place the application in condition for allowance and early, favorable action is respectfully solicited.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to Deposit Account No. 50-0911.

Respectfully submitted,

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